

CLAIMS

What is claimed is:

- Sub B1
- 1 1. A display device comprising:
2 an array of display drivers, said display drivers including a first plurality of
3 display drivers, wherein said display drivers control the display of a
4 plurality of pixels in a display area and wherein said display drivers are
5 located within said display area which is viewable;
6 said first plurality of display drivers comprising a first serial shift register
7 having a first plurality of memory elements each corresponding to and
8 coupled to one display driver of said first plurality of display drivers.
- 1 2. A display device as in claim 1 wherein display data for pixels in a first row of
2 pixels are stored in said first plurality of memory elements and wherein said plurality
3 of pixels are a two-dimensional array of pixels.
- 1 3. A display device as in claim 2 wherein a second plurality of display drivers
2 comprise a second serial shift register having a second plurality of memory elements
3 each corresponding to and coupled to one display driver of said second plurality of
4 display drivers.
- 1 4. A display device as in claim 2 wherein said display drivers drive pixel
2 electrodes which control a display medium which comprises one of (a) a liquid crystal

1 11. An integrated circuit (IC) device comprising:

2 a substrate which includes an integrated circuit;
3 a plurality of functionally symmetric interface pads coupling said integrated
4 circuit to a receptor site of an electronic device, said plurality of
5 interface pads being arranged in said substrate such that said electronic
6 device operates with said substrate mounted to the receptor site in any
7 one of a plurality of orientations relative to said receptor site, and
8 wherein said integrated circuit comprises:
9 an instruction decoder coupled to at least one of said plurality of
10 interface pads, said instruction decoder decoding an instruction
11 received through said at least one of said plurality of interface
12 pads and causing an operation of said integrated circuit.

1 12. An IC device as in claim 11 wherein said integrated circuit further comprises:
2 an instruction register coupled to said instruction decoder for storing said
3 instruction;
4 a control bus coupled to said instruction register.

1 13. An IC device as in claim 11 wherein said instruction decoder further
2 comprises:
3 a timing discriminator coupled to said at least one of said plurality of interface
4 pads said timing discriminator discriminating between clocking signals
5 and instruction data which represent said instruction.

1 15. An IC device as in claim 14 wherein said IC device is a display driver and
2 wherein said plurality of instructions cause said display driver to control at least one
3 pixel of a display.

1 16. An IC device as in claim 11 wherein said integrated circuit further comprises:
2 a shift register coupled to at least one of said plurality of interface pads, said
3 shift register shifting data stored in said shift register under control of
4 said instruction.

1 17. An IC device as in claim 11 wherein said integrated circuit further comprises:
2 a position detector coupled to at least one of said plurality of interface pads,
3 said position detector detecting a position of said integrated circuit
4 relative to said receptor site.

1 18. An IC device as in claim 17 wherein said position detector provides a signal
2 which is determined by said position.

1 19. An IC device as in claim 11 wherein said at least one of said plurality of
2 interface pads provides both said instruction to said instruction decoder and clock
3 signals for controlling clocked operations of said integrated circuit.

- 1 20. An integrated circuit (IC) comprising:
2 a semiconductor substrate having a plurality of pads for electrical interconnect
3 to other circuitry;
4 a position detector coupled to at least one of said pads of said plurality of pads,
5 said position detector detecting a position of said IC relative to a
6 receptor substrate and providing a signal, internally within said
7 semiconductor substrate, which is determined by said position.
- 1 21. An IC as in claim 20 wherein said position comprises at least one of a
2 translational location on said receptor substrate or a rotational orientation of said IC
3 relative to said receptor substrate.
- 1 22. An IC as in claim 20 wherein said plurality of pads comprises a first pad
2 which is configurable depending upon said signal.
- 1 23. An IC as in claim 22 wherein said first pad is configurable as one of (a) an
2 input pad, or (b) an output pad, or (c) a no-operation pad.
- 1 24. An IC as in claim 20 wherein at least one function of said IC is determined by
2 said signal.

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1 25. An IC as in claim 20 wherein said IC is capable of performing at least one of a
2 plurality of functions and wherein said signal causes said IC to perform a selected
3 subset of said plurality of functions.

1 26. An IC as in claim 20 wherein said position is specified by a conductive layer
2 on said receptor substrate which makes electrical contact with said position detector
3 through said at least one of said pads.

1 27. An IC as in claim 25 wherein said selected subset is determined by a
2 conductive layer on said receptor substrate which makes electrical contact with said
3 position detector through said at least one of said pads.

1 28. An integrated circuit (IC) comprising:
2 a semiconductor substrate having a plurality of pads for electrical
3 interconnection to other circuitry;
4 a position detector coupled to at least a first pad of said plurality of pads, said
5 position detector detecting a position of said IC relative to a receptor
6 substrate, wherein said first pad is configurable as at least one of the
7 following: an input pad or output pad or a no-operation pad as
8 determined by said position.

1 29. An IC as in claim 28 wherein said position comprises at least one of a
2 transitional location on said receptor substrate or a rotational orientation of said IC
3 relative to said receptor substrate.

1 30. An IC as in claim 28 wherein said position detector provides a signal which
2 causes said first pad to be configured and wherein said first pad is configurable as one
3 of at least two of the following: an input pad or an output pad or a no-operation pad
4 as determined by said position.

1 31. An IC as in claim 28 wherein said position is specified by a conductive layer
2 on said receptor substrate which makes electrical contact with said position detector.

1 32. An assembly comprising:
2 a receptor substrate having a conductive layer disposed over at least a portion
3 of said receptor substrate;
4 an integrated circuit (IC) having a plurality of pads for electrical interconnect to
5 other circuitry, said IC having a position detector coupled to at least
6 one of said pads which is coupled to said conductive layer, said
7 position detector detecting a position of said IC relative to said receptor
8 substrate and providing a signal which is determined by said position.

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34. An assembly as in claim 32 wherein said position comprises at least one of a translational location on said receptor substrate or a rotational orientation of said IC relative to said receptor substrate.

1 36. An IC as in claim 35 wherein said first pad is configurable as one of (a) an
2 input pad, or (b) an output pad, or (c) a no-operation pad.

1 38. An IC as in claim 32 wherein said IC is capable of performing at least one of a
2 plurality of functions and wherein said signal causes said IC to perform a selected
3 subset of said plurality of functions.

1 42. An integrated circuit device comprising:
2 a substrate which includes an integrated circuit (IC);
3 a plurality of functionally symmetric interface pads coupling said IC to a
4 receptor site of an electronic device, said plurality of interface pads
5 being arranged in said substrate such that said electronic device
6 operates with said substrate mounted to the receptor site in any one of a
7 plurality of orientations relative to said receptor site, wherein said
8 plurality of interface pads comprises:
9 a reference voltage pad for receiving a reference voltage signal;
10 a power supply pad for receiving a power supply signal;
11 at least four output pads;

12 a first configurable pad which is configurable as one of at least two of
13 the following: an input pad or an output pad or a no-operation
14 pad;

15 a second configurable pad which is configurable as one of at least two
16 of the following: an input pad or an output pad or a no-
17 operation pad.

1 43. An IC device as in claim 42 wherein said reference voltage signal is ground
2 and wherein said plurality of interface pads further comprise:

3 a clock pad for receiving a clock signal for controlling clocked operations of
4 said IC;

5 a third configurable pad which is configurable as one of at least two of the
6 following: an input pad, or an output pad or a no-operation pad;

7 a fourth configurable pad which is configurable as one of at least two of the
8 following: an input pad, or an output pad or a no-operation pad;

9 four position indicator pads.

1 44. An IC device as in claim 43 wherein said plurality of interface pads comprise
2 up to 25 pads arranged in an array up to 5×5 and wherein there are four reference
3 voltage pads and four power supply pads and eight output pads.

1 45. An assembly comprising:

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2 a receptor substrate having a conductive layer disposed over at least a portion
3 of said receptor substrate;
4 an integrated circuit (IC) attached to said receptor substrate and having a
5 plurality of interface pads, including at least one interface pad which is
6 coupled to said conductive layer to receive a signal from said
7 conductive layer, said IC also comprising:
8 a first logic circuit coupled to a first set said interface pads and
9 providing a first function;
10 a second logic circuit coupled to a second set of said interface pads and
11 providing a second function which is different than said first
12 function;
13 a selector logic circuit coupled to said first logic circuit and coupled to
14 said second logic circuit and coupled to receive said signal
15 which causes said selector logic to select between said first
16 function and said second function such that said IC performs
17 only one of said first and said second functions.

1 46. An assembly as in claim 45 wherein said IC is attached to said receptor
2 substrate through a fluidic self-assembly process, and wherein said first set and said
3 second set of interface pads overlap at least partially.

1 47. An assembly as in claim 45 wherein said signal is determined by a position of
2 said IC on said receptor substrate.

1 52. An assembly comprising:
2 a receptor substrate having an opening and a substantially planar region
3 surrounding said opening and having a plurality of conductive layers
4 attached over said substantially planar region;
5 an integrated circuit (IC) attached to said opening in said receptor substrate,
6 said IC having electrical interface pads on a substantially planar surface
7 which is substantially co-planar with said substantially planar region,
8 said IC further comprising:
9 a first logic circuit coupled to a first set of said electrical interface pads
10 and providing a first function;

1 53. An assembly as in claim 52 wherein said IC is attached to said receptor
2 substrate through a fluidic self assembly process, and wherein said first set and said
3 second set of electrical interface pads overlap at least partially.

1 55. An assembly as in claim 52 wherein said IC is capable of performing both said
2 first function and said second function substantially concurrently.

1 56. An integrated circuit (IC) comprising:
2 an instruction data logic coupled to an electrical interface pad, said instruction
3 data logic receiving instruction commands to cause said IC to perform
4 a particular function depending on a received instruction command;
5 a clocked logic circuit coupled to said electrical interface pad, said clocked
6 logic circuit receiving a clock signal through said electrical interface
7 pad which also provides said instruction commands to said IC.

1 57. An IC as in claim 56 further comprising:

1 61. A circuit as in claim 60 wherein said voltage value is a voltage rail supplying
2 power to said logic.

68. A display device comprising:
a two-dimensional (2-D) array of pixels;
an array of display drivers which are coupled to and which control said 2-D
array of pixels, each of said display drivers receiving a clock signal

1 69. A display device as in claim 68 wherein data in said data signal is shifted
2 through said display under control of said clock signal.

70. A display device as in claim 68 wherein said display device comprises an active matrix backplane which includes said array of display drivers and wherein circuitry in said active matrix backplane including said array of display drivers, are interconnected with only a single electrically conductive interconnection layer which is attached to and disposed over said active matrix backplane.

71. A circuit for shifting a voltage level of a signal, said circuit comprising:
a first input to receive a clocked signal having a pulse during each clock cycle;
a second input to receive a first voltage signal;
a current mirror circuit coupled to said first input and coupled to said second input, said current mirror controlling a state of a node;
an output driver coupled to said node, said output driver shifting said first voltage signal to a second voltage signal when said node is at a first state.

1 72. A circuit as in claim 71 wherein said current mirror circuit comprises:
2 a first current path;

73. A circuit as in claim 72 wherein said first control electrode is a first gate electrode of a first transistor device which is in said first current path and wherein said second control electrode is a second gate electrode of a second transistor device which is in said second current path and wherein said node is in said second current path and wherein said first transistor device and said second transistor device have respectively first and second size parameters which are substantially matched.

1 74. A circuit as in claim 73 wherein said pulse causes a current to flow in said
2 second current path to set said node at said first state and wherein after said pulse, said
3 node retains said first state with substantially no current flowing in said second current
4 path.

75. A method for operating a circuit for shifting a voltage level of a signal, said method comprising:

- receiving a first voltage signal;
- receiving a clocked signal having a pulse during each clock cycle;
- passing current through a first current path and a second current path which together form a current mirror, said current being passed when said

76. A method for operating a circuit for shifting a voltage level of a signal, said method comprising:

- receiving a first voltage signal;
- receiving a clocked signal having repetitive clock cycles, each clock cycle having a corresponding pulse;
- passing a current through a node during a first pulse of a first clock cycle to set said node at a first state, said node floating at substantially said first state during said first clock cycle after said first pulse;
- driving an output to a second voltage signal from said first state of said node.

1 77. A method as in claim 76 wherein said driving occurs while said node is
2 floating.

1 78. A method as in claim 77 wherein said floating occurs by disconnecting said
2 node from power and ground reference voltage rails.

1 79. A circuit for shifting a voltage level of a signal, said circuit comprising:
2 a first input to receive a clocked signal having a pulse during each clock cycle;

3 a second input to receive a first voltage signal;
4 a driving node coupled to said first input and coupled to said second input,
5 said driving node floating when said pulse is not present in a
6 corresponding clock cycle;
7 an output driver coupled to said driving node, said output driver shifting said
8 first voltage signal to a second voltage signal when said node is at a
9 first state.

1 80. A circuit as in claim 79 wherein said output driver comprises an output
2 transistor and said driving node is coupled to a control electrode of said output
3 transistor.

1 81. A circuit as in claim 80 further comprising a current mirror circuit having a
2 first current path coupled to a second current path and wherein said driving node is in
3 said second current path.

1 82. A display device comprising:
2 a two-dimensional (2-D) array of pixels;
3 an array of display drivers which are coupled to and which control said 2-D
4 array of pixels, each of said display drivers receiving a data signal,
5 wherein said data signal is bussed only substantially parallel to one
6 axis of said display and wherein said display device comprises an
7 active matrix backplane which includes said array of display drivers

1 83. A display device as in claim 82 wherein said pixels of said 2-D array of pixels
2 is not arranged in rows and columns.